

REMARKS

Claims 1-3, 6-8, 11 and 12 are pending in the present application. Claims 11-3, 6-8, 11 and 12 stand rejected. Claims 1 and 8 are amended herein. No new matter is introduced as a result of the claim amendment. The Examiner's rejections are traversed below. Applicants respectfully request the Examiner to consider and allow the remaining claims.

Claim Rejections – 35 USC § 103

Claims 1-3, 6-8, 11, and 12 stand rejected under 35 USC 103(a) as being unpatentable over Mehrad et al. (U.S. Patent No. 6,765,257; hereinafter “Mehrad”) in view of Ito et al (U.S. Patent No. 6,700,176; hereinafter “Ito”).

Claims 1 and 8 have been amended herein to recite *erasable* memory cells. Ito does not teach an erasable memory cell. Rather, Ito teaches an *antifuse* structure. Applicants understand an antifuse to be an electrical device that performs the opposite function of a fuse. In other words, an antifuse starts with a high resistance and is designed to permanently create an electrically conductive path (i.e., short-circuit) when the voltage at the gate of the antifuse exceeds a certain level. In other words, the anti-fuse of Ito only allows for a *one-time program*. Indeed, Ito describes in detail how the antifuse device is “normally an open circuit until a programming current is forced through the gate ... [causing] the antifuse device 300 to break down or ‘blow’ ... [and] act as a short-circuit.” Ito, col. 5, lines 43-50. Applicants respectfully submit that the one-time programmable antifuse of Ito teaches away from the erasable memory cells recited in Claims 1 and 8.

Notwithstanding the above arguments, Applicants respectfully submit that the Examiner has not made a sufficient showing of a motivation/suggestion to combine the Mehrad and Ito references. Referencing column 6, lines 46-49 of Ito, Examiner states that “Ito discloses reduced on-state resistance and improved current characteristics.” However, in using this language as the basis for his motivation to combine, Applicants respectfully submit that Examiner has unfairly ignored essential language in the cited portion. In particular, Ito states that its antifuse device exhibits these characteristics “*when blown*.” Ito, col. 6, lines 46-49. In other words, these characteristics do not arise until the device has “blown” (i.e., until has been applied to the gate oxide that causes it to physically rupture). Applicants respectfully submit that one of skill in the art desiring to make an erasable memory cell would not be motivated to consult the teachings of a reference that teaches the physical rupturing of the gate oxide. Moreover, this *specifically teaches away* from source and drain implantation regions being able to conduct independent of any voltage applied to a stacked gate structure, as recited in Claim 8.

Furthermore, Ito states that the rupturing of gate oxide shorts a portion of the gate to the underlying channel, thereby providing low resistance *between the gate* and the drain, source, substrate, etc. Specifically, Ito does not mention any potential improvements in current characteristics between the drain and source. More to the point, Ito neither teaches nor suggests using a drain, by way of a diffused source/drain region, to couple a common source line to a source contact that is disposed in a row of drain contacts, as claimed.

It is respectfully submitted that Mehrad cannot overcome the cited shortcomings of Ito. Thus, Applicants respectfully assert that the rejection of claims 1 and 8 under 35 U.S.C. 103(a) as being unpatentable over Mehrad in view of Ito is

traversed, and that claims 1 and 8 are now in condition for allowance. Claims 2, 3, 6 and 7 are dependent on claim 1 and recite additional limitations. Claims 11 and 12 are dependent on claim 8 and recite additional limitation. Therefore, Applicants assert that the rejection of claims 2, 3, 6, 7, 11 and 12 is also traversed, and that claims 2, 3, 6, 7, 11 and 12 are in condition for allowance as being dependent on allowable base claims.

CONCLUSION

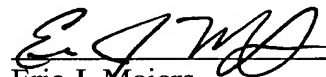
In light of the response presented herein, Applicants respectfully assert that Claims 1-3, 6-8, 11 and 12 of the present application overcome the rejections of record, and therefore earnestly solicit allowance of these claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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